DESIGN RULE CHECK TO VALIDATE OPTION METAL AND VIA FOR A PREPROGRAMMED LAYOUT DESIGN

By

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A Dissertation submitted for partial fulfilment of the requirement for the degree of Master of Science

July 2014

Acknowledgement

Designing the algorithm to check the option metal and via had been the pinnacle of my life in learning and gain enormous knowledge. Through this project I have gained a great skills and experience in designing Design Rule Check algorithms for verification by doing research and simulations.

I also would like to take this opportunity to express my sincere gratitude to my supervisor Dr. Asrulnizam Abd Manaf for his time, support, encouragement and guidance through this project phase. Without his guidance and generosity in imparting his knowledge and experience had become a tremendous approach towards completing each phase of this project.

Besides, I would like to extend my sincere thankfulness to my supervisor in Altera, Mr Eric Leong, who guide me through the completion of the project. He also had been very supportive and encouraging in the process of completing the final phase of the project.

Lastly, I like to thank my family, friends and USM staff who shared their love, encouragement and never ending support throughout all situation of happy and obstacles faced.

Table of Contents

List of Tables

List of Figures and Illustrations

List of Abbreviations and Nomenclature

Abbreviation	Meaning
ACA	Ant Colony Algorithm
ALADIN	Automatic Layout Design Aid for Analogue Integrated Circuit
CAD	Computer Aided Design
CAE	Computer Aided Engineering
ChipDRE	Chip Level Design Rule Evaluator
CMOS	Complementary Metal-Oxide Semiconductor
DRE	Design Rule for Evaluation
DA	Design Automation
DFM	Design For Manufacturability
DFT	Design For Testability
DPT	Double Patterning Technology
DR	Design Rule
DRC	Design Rule Check
DRE	Design Rule Evaluator
EDA	Electronic Design Automation
ESD	Electrostatic Discharge
FIB	Focused Ion Beam
FPGA	Field Programmable Gate Arrays
GCPW	Good Chip Per Wafer
GDR	Global Design Rules
GDS	Graphic Database System
HP	High Performance
IC	Integrated circuit
ILD	Interlayer Dielectric
I/O	Input/output
LDR	Local Design Rules
LI	Local Interconnects
LLDFT	Layout Level Design For Testability
LVS	Layout versus Schematic
LVTTL	Low Voltage Transistor-transistor Logic Level
NMOS	N-type Metal Oxide Semiconductor Logic
PCB	Printed Circuit Board
PLD	Programmable Logic Devices
PLL	Phased Lock Loop
PMOS	P-type Metal Oxide Semiconductor Logic
RDR	Restrictive Design Rules
ROM	Read Only Memory
SLP	Super Low Power
SoC	System on Chip
SSTL	Stub Series Terminated Logic
SVRF	Standard verification Rule Format
TSMC	Taiwan Semiconductor Manufacturing Company
TTL	Transistor-transistor Logic
VLSI	Very Large Scale Integration

Abstrak

Transistor diskala pada skala kecil untuk meningkatkan bilangan transistor dalam sebuah cip tunggal dan menyumbang kepada variasi blok IP. Justeru itu, rekabentuk susun atur menjadi kompleks dan proses mengesahkan rekabentuk susun atur akan menjadi semakin mencabar. Penggunaan lapisan pilihan telah dikenal pasti di mana ia akan mempunyai satu litar dan susun atur asas. Selepas susun atur selesai direka, ia adalah sangat mudah untuk menukar logam dan lubang hubung pilihan kepada logam dan lubang hubung sebenar. Walau bagaimanapun, pengesahan konvensional menggunakan peraturan rekabentuk (DRC) di CADENCE tidak meliputi pemeriksaan pada lapisan pilihan. Lapisan pilihan pada susun atur yang diprogramkan tidak disahkan betul dan boleh menyebabkan ralat. Projek ini akan membolehkan pengesahan lapisan pilihan dengan membangunkan satu algoritma yang dapat meliputi pemeriksaan untuk kedua-dua lapisan pilihan dan sebenar bagi logam dan lubang hubung. Projek ini adalah berdasarkan pada proses 20nm TSMC dan pengubahsuaian dibuat bagi membolehkan pemeriksaan pada lapisan pilihan. Pengubahsuaian dibuat dengan cepat dan pemeriksaan kes terburuk dapat dilakukan melaui proses automasi kod dengan mengunakan Pengekstrakan praktikal dan Laporan Bahasa (PERL). Hasilnya ditunjukkan dengan melukis corak ujian dengan peraturan rekabentuk. Contohnya, jika satu peraturan dengan spesifikasi lebih daripada atau sama dengan 0.05nm dilukis pada spesifikasi kurang daripada 0.05nm akan menyebabkan ralat. Pendekatan ini telah digunakan bagi semua peraturan reka bentuk yang terlibat dalam teknologi proses 20nm. Kaedah yang dicadangkan untuk mengesahkan lapisan pilihan berjaya dan kesilapan yang paling kerap berlaku pada peringkat awal merekabentuk susun atur dapat dikurangkan.

Abstract

Transistor sizing had been scaled down to increase the number of transistors in a single chip which also leads to the variation of IP blocks. Consequently, the layout design becomes very complex and it is challenging to verify the layout design. Therefore, the option layer had been identified where it will have a common base circuitry and layout. After the layout is completed, it is very convenient to convert the option metal and via to real metal and via layer. However, the conventional verification using the design rule check (DRC) in Cadence does not include the check for option layer. Option layer on preprogrammed layout are not verified correct and may cause a violation. Thus, this project will enable the verification of the option layer by developing an algorithm which able to cover the check for both option and real metal/via layer. This project will be based on TSMC 20nm process library and the modifications are made to enable the option layer check. In order to enable the modification to be made quickly and enable worst case check, Practical Extraction and Report Language (PERL) programming used to automate the code. The result is shown by drawing the test pattern with design rule. As example, a rule with specification of more than or equal with 0.05nm will flag an error if the test pattern is drawn less than 0.05nm. This approach had been applied to all the design rules involved in 20nm process technology. The method proposed validates the option layer successfully and most errors found in the early stage of designing the layout are minimized.

CHAPTER 1

INTRODUCTION

1.1 Introduction

The invention of the integrated circuit (IC) by Jack Kilby in 1958 had contributed to the advancement of technology. Integrated circuit (IC) technology has become the fundamental technology towards the development of the innovative devices and systems. The past decades have seen how these small silicon chips gradually prevail and play an indispensable role in our life. ICs can be found in almost every electronic device designed in the new era.

The process of developing IC manufacturing process had never stop from meeting the increasing demands for new products with higher performance and strong functionality. As the feature size scales down, a single transistor runs faster and consumes less power.

IC designers are able to pack more transistors into a single chip and make the chip more powerful. The trend of increasing number of transistors follows Moore's law, who predicts that the number of transistors being packed into a single integrated circuit doubles around every 18 months. This law had been carried out till today, where the ICs are designed at 14nm process technology. Besides, this integration

allowed us to build systems with more transistors by allowing more computing power to be applied to solve a problem.

Integrated circuits are also easier to be designed, manufactured and are more reliable than discrete systems. However, as the size of the transistor shrinks into nanometer scale, it becomes a challenge for IC manufacturer to achieve both good manufacturability and cost efficiency. Apart from that, IC manufacturers also face many challenges in the more sophisticated manufacturing process which includes, increasing circuit complexity, sub-wavelength lithography, and use of new materials for interconnect and dielectric (Antonsson, 2003) (Kai-Ti Hsu, 2012) (Tseng-Chin Luo, 2012) (Wolf, 2008).

1.2 Problem Statement

Most of the fabless companies are involved in the process of designing ICs for various usages. They use various designing tools to automate the design and validate the design process. The custom mask layout is designed based on the rules and parameters provided by foundry. After the designing process is completed, an algorithm is developed to validate the mask layout. The algorithm was developed from the Standard Verification Rule Format (SVRF) and foundry technology. This algorithm helps to verify the mask layout in order to prevent any Design Rule Check (DRC) violation.

Most of the mask layouts are predesigned with option metal and via to ease the layout designing process. The option layer is converted from option to real from time to time until the final design is completed. However, current preprogrammed mask layout with option layer does not include the Design Rule Check (DRC) for option layer. Therefore, the predesigned location for option metal and via is not verified to be correct and might cause error when converted to real layer. Consequently, this will cause the preprogrammed mask layout to be redesigned in order to meet the layout designer's design requirement.

By creating a design rule for the preprogrammed mask layout with the ability to check the optional layer before the real placement could be a solution for this problem. Moreover, this design rule check can be a medium to facilitate the exact position of metal/via without causing any DRC violation. Furthermore, the preprogrammed mask layout can be used as a template for most of the design to cut the cost of production. Since there is no specific rule for the placement of via and metal in the preprogrammed layout at the early stage of design, the validation of the design process is very time consuming and can increase the cost of production.

Besides, the proposed modified algorithm for the option via/metals can contribute towards the validation of the overall design before the placement of via/metal and make the fabrication process much faster.

1.3 Project Objective

The main objective of this project is:

a) To develop an algorithm which is able to check both option metal and option via along with real metal and via.
b) To validate the developed algorithm by testing for the worst case.
c) To develop a Practical Extraction and Report Language (PERL) program to enable the modification to be made to runset level.

1.4 Project Scope

This research is done based on Taiwan Semiconductor Company (TSMC) 20nm process technology. The design rule is referred from TSMC and the algorithm is being modified based from the existing algorithm. The research is being done within Altera organization to improve the design automation process to a new level of validation process.

1.5 Outline of Project Report

The project is organized through five chapters including first chapter.

Chapter 2 focuses on project's literature review which establishes the academic and research areas related to the project obtained from various sources which includes

books, journals and articles. This chapter further explains the need for Design Rule Check, the importance of optional layer and previous works related to DRC. Besides, it also explains some of the commands used in the process of developing the algorithm. Chapter 2 also provides details on previous works related to DRC. Chapter 2 also serves as a guide and reference for the methodology in Chapter 3.

Chapter 3 is devoted to the project methodology. Methodology includes a discussion of both theoretical issues and practical matters of data collection. The procedures for the overall project methodology and simulation design methodology are expressed with flow charts. Furthermore, this chapter includes brief summary of the information gathered and studied in Chapter 2.

In Chapter 4, a detailed explanation about the finding and analysis of the project, this includes the simulation results and the problems encountered throughout the duration of the project. The results are shown in tables, compared and observed thoroughly.

The Chapter 5 gives an overall conclusion of the project and further recommendation for the project. This chapter summarize the overall work has been done, observed and discovered throughout the project. It also states the project's objectives have been achieved. Moreover, from the limitations faced by the project, recommendations to further improve the project are given.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Integrated circuit (IC) layout designs have a large number of polygons where it represents different layer of masks. Layout verification determines whether these polygons in a very large scale integration (VLSI) chip comply with all technology requirements. The increasing design complexity and the number of polygons in the different mask layers in a VLSI chip are increasing drastically from time to time.

The processing of the design layout is very time consuming in the layout verification due to the large number of polygons in an IC design. Design Rule Check (DRC) is commonly used to verify a layout design and detects manufacturing rule violations such as width, spacing, and length rules. In reducing the level of process variability, physical-design techniques have been proposed to improve the original IC layout to improve manufacturability (B.W. Lindsay, 1975). The design rule checks (DRC), equation based DRC, layout versus schematic comparison (LVS) and parasitic extraction are provided by the verification tools (Graphics, 2013).

2.2 Brief History

For the past two decades, the electronics industry has grown very drastically both in size and complexity. At early stage of chip design is only to reduce the computer size. However, the reduce size is now being a fundamental measure for computer speed.

Originally, IC layout design was hand-drafted on special paper called Mylar. Due to the market demands and advances in technology brought about an immediate need to develop software and hardware solutions to cater the time-to-market of the chip designs and to automate the entire process. Accuracy of the final masks was also the main concern in the process of computerization of layout design. The very early platforms were custom built to ensure that graphics applications ran quickly and had sufficient capabilities. CALMA (Data General) built main-frame-sized machines and developed specialized software for printed circuit board (PCB) and integrated circuit (IC) applications.

The enormous revolution in hardware was the development of the “engineering workstation,” which ran a version of the UNIX platform. As the hardware platform growth, the software development progressed even faster as indicated by the growing technology. Mentor Graphics, Cadence, Compass and Daisy which gained larger shares of the IC and PCB design tools market.

Towards, upgrading of the software, more automation of the tasks that was labour intensive had been introduced. The significant example of automation includes:

Layout synthesis: Instead of the conventional methods of manually drawing polygons, layout designs can be created from "code".

Layout migration: By using mapping and sophisticated compaction techniques layouts can be moved from one set of design rules to another.

Layout verification: Is the tool used to perform design rule checks on the final layout before it sent for production.

Circuit synthesis: Schematics can be automatically generated by using VHDL or Verilog. As more circuitry being produced by this circuit synthesis tools, layout automation such as place-and-route tools had been very essential.

Place-and-route: Optimizing the placement for minimum connectivity, instance placement for literally millions of cells and maximum circuit performance.

The changes make this industry very interesting to be involved. However, the fundamental concepts involved in producing quality layout are based on physical and electrical properties that never change (Clein, 2000).

2.3 Layout Design

Layouts are designed based from transistors, wires and vias. On either side of the gate polysilicon, the P and N bulk regions are defined by diffusing areas. The substrate, contacts and guard rings (other active areas) are formed at the same time. Contact holes are created in the isolation layer on top of the layer, to enable the interconnect layers to be connected to the polysilicon and/or active areas. The interconnect layers fill the contact holes which was created in the previous step. The final layer is known as the passivation layer with openings for wire bonding

connections. The passivation layer is a glass layer that separates the chip from the external world (Clein, 2000) (Wolf, 2008).

2.3.1 Layers and connectivity

In most CMOS process, there are four basic layer types. This includes conductors, isolation layers, contacts or vias and implant layers.

1. **Conductors**: Conducting layers such as diffusion areas, metal and polysilicon layers that are able to carry signal voltages.
2. **Isolation layers**: Insulator layers which isolate each conductor layer from each other in vertical and horizontal direction to avoid “short circuits” between separate electrical nodes.
3. **Contacts or vias**: This layer includes metal and via, where it cuts in the insulation layer that separates conducting layers. It also allow the upper layer to contact down through the cut or “contact” hole.
4. **Implant layers**: These layers customize or modify existing conductor propriety but do not define a new layer or contact.

These four types of layers are used to create transistor devices, resistors, capacitors and interconnections (Clein, 2000).